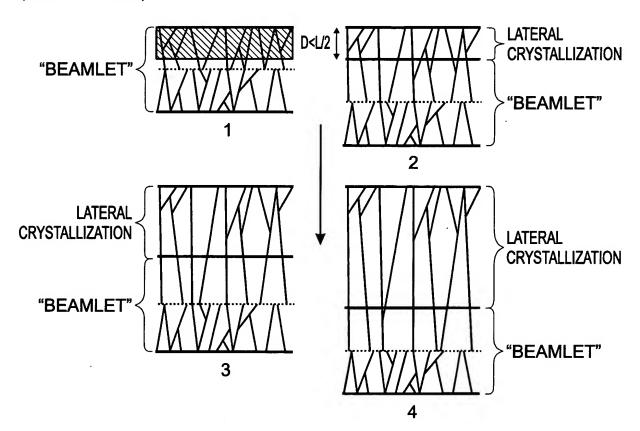
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Fig. 1 (PRIOR ART)



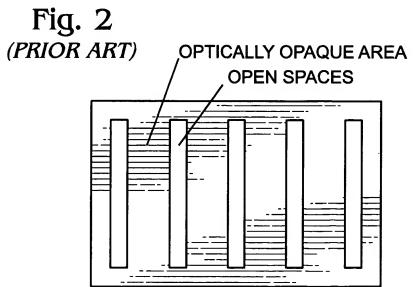
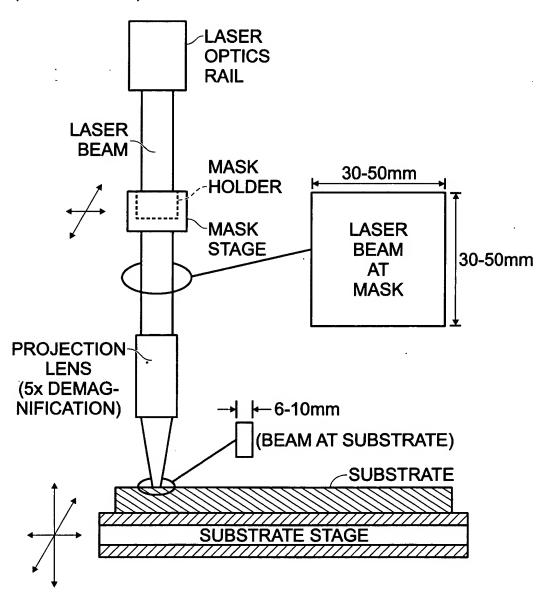
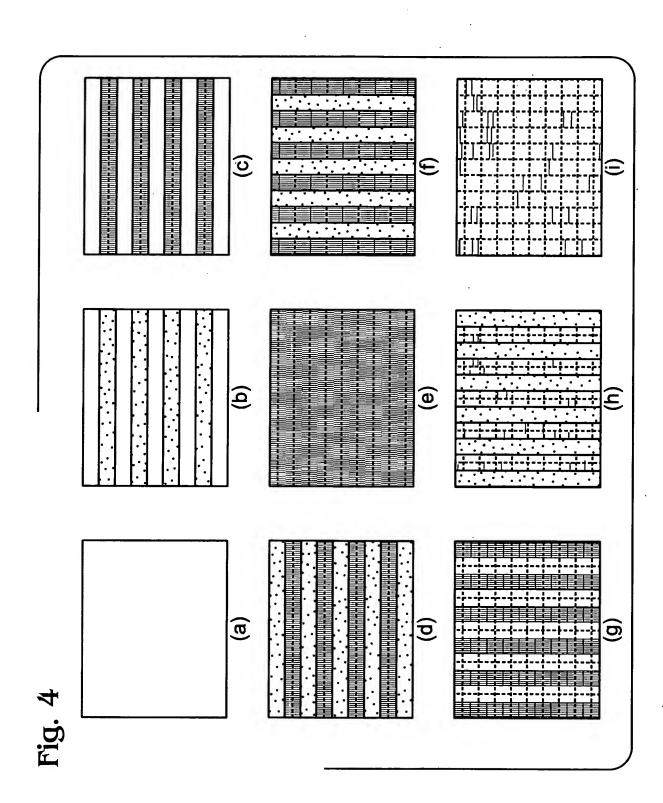


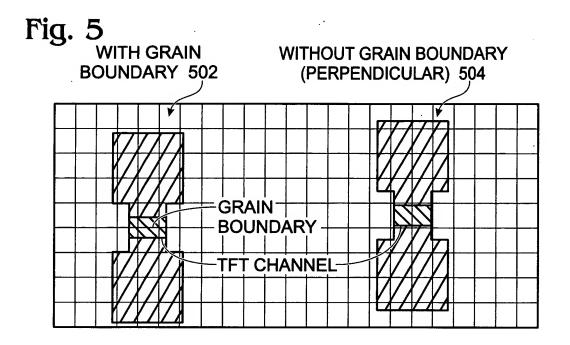
Fig. 3 (PRIOR ART)

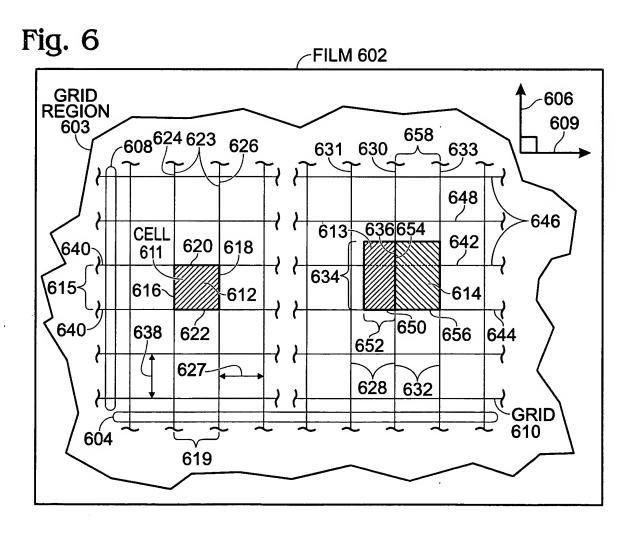


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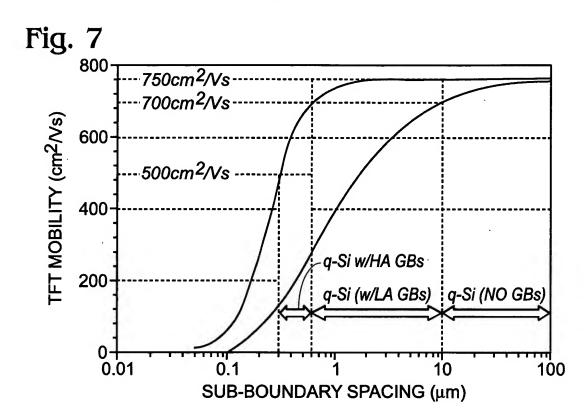


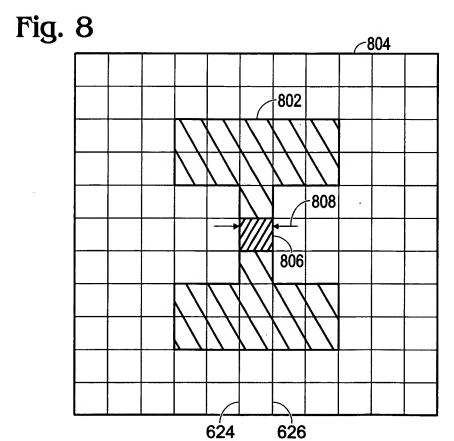
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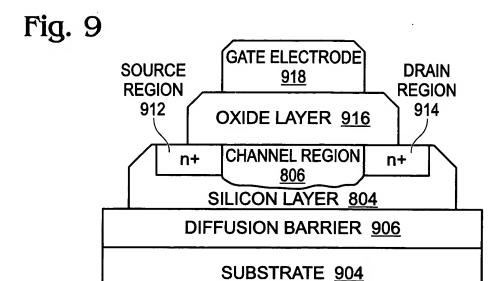


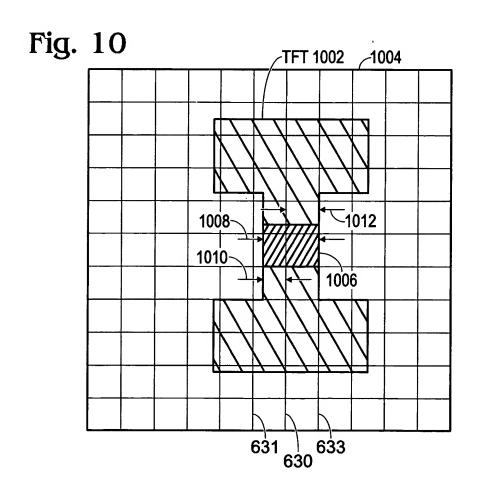


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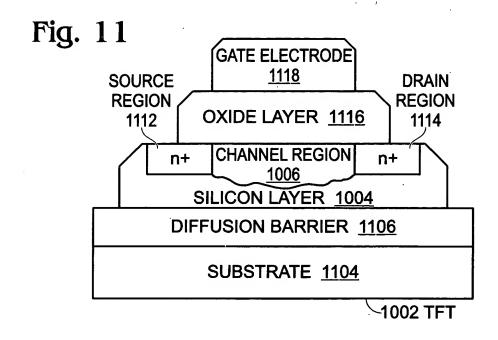


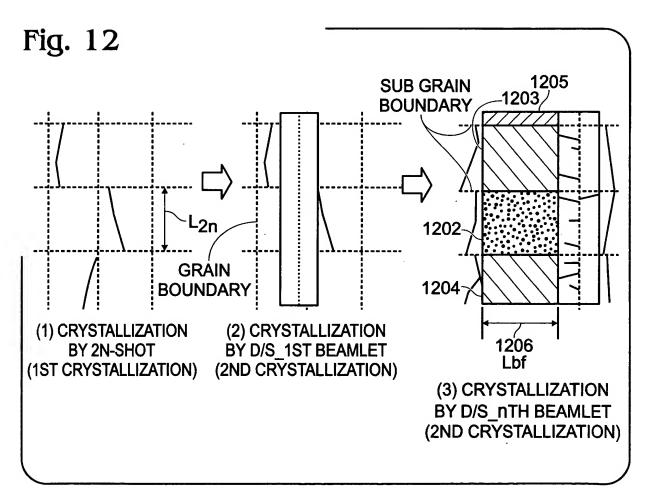


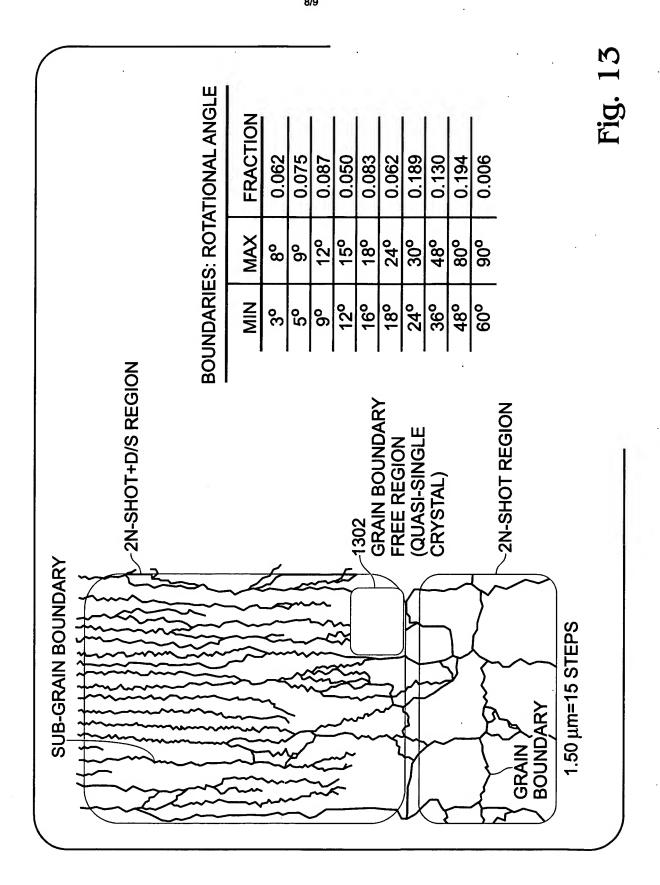




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Fig. 14	ST	1400	
	,	<u></u>	-1401
	FORMING A TRANSPAR	ENT SUBSTRATE LAYER	
		\ \ 	-1402
	FORMING A DIFF	FUSION BARRIER	
	\		<u> 1403</u>
	FORMING A FILM OF	AMORPHOUS SILICON	
		· /	<u> 1404</u>
		ER PROCESS TO FORM LLINE SILICON	
	\	<u>l</u>	<u> 1407</u>
EXPOSING	G THE FIRST AREA TO A	N ADDITIONAL ENERGY SOUR	CE
		<u>.</u>	<u>-1410</u>
	TION, THROUGH THE FI	R BEAM, IN TWO STEPS PER RST AND SECOND APERTURE ALING THE FIRST AREA	
		<u>.</u> V	<u> 1414</u>
		RTHOGONAL FIRST AND SECO RIDGED, GRAIN BOUNDARIES	ND
		<u>I</u> . ✓	<u>-1416</u>
SELEC	TING A SECOND AREA,	INCLUDED IN THE FIRST AREA	
[···	7		<u>-1418</u>
USING DIRE	CTIONAL SOLIDIFICATI	ON TO ANNEAL THE SECOND A	
EVECUIVE	THE OF COLOR & DEA TO		<u>-1419</u>
EXPOSING	THE SECOND AREA TO	AN ADDITIONAL ENERGY SOU	
LICINIC A	I ACED TO SECUENTIAL	Y LLY ANNEAL THE SECOND ARE	<u>~1422</u>
USINGA	LASEN TO SEQUENTIA	LLY ANNEAL THE SECOND ARE	
SELECTIVE!	Y REMOVING GRAIN BOI	UNDARIES AND SMOOTHING RID	-1424 GES
COLLEGIALE	TI TICIAIO A II 10 OI OAII 1 DOI		-1426
FORM	ING A TRANSISTOR CH	ANNEL IN THE SECOND AREA	71420
	7	7	-1428
FORMIN	NG SOURCE AND DRAIN	REGIONS IN THE FIRST AREA	
	7	7	-1430
	FORMING A GATE (DIELECTRIC LAYER	
	7	7	-1432
FORMING A	A GATE ELECTRODE OV	ERLYING THE DIELECTRIC LAY	'ER